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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,290	03/31/2006	Mitsuaki Osame	0756-7670	7471
31780	7590	01/06/2009	EXAMINER	
ERIC ROBINSON			NGUYEN, LONG T	
PMB 955			ART UNIT	
21010 SOUTHBANK ST.			PAPER NUMBER	
POTOMAC FALLS, VA 20165			2816	
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			01/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/574,290

Applicant(s)

OSAME ET AL.

Examiner

LONG NGUYEN

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) 7-18 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-6 and 19-21 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 24 June 2008 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/S5108)
Paper No(s)/Mail Date 3/31/06
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election of specie 1B, claims 1-6 and 19-21 in the reply filed on 10/30/08 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Note that claims 7-18 are currently withdrawn from consideration.

Drawings

2. The drawings are objected to because Figures 20A-20B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 19 and 20 are objected to because of the following informalities:

For claim 19, "a potential" on line 6 should be changed to --the third potential-- to avoid a confusion in the claim since the claim already recited the circuit generates a third potential (see claim 1, line 7, or claim 3, line 7).

For claim 20, “a potential” on line 6 should be changed to –the respective third potential and fourth potential-- for the similar reason as discussed in claim 19 above (also see claim 5, lines 8 and 10).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al. (USP 5,198,699).

With respect to claims 1, 2 and 21, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (P-channel transistor 96), a first power source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground); and a circuit (130, 134) for applying a third potential (Vy) which is different from the first potential and the second potential; a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims.

With respect to claims 3, 4 and 21, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (N-channel transistor 90), a first power

source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground); and a circuit (114, 116) for generating a third potential (Vx) which is different from the first potential and the second potential; a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims.

With respect to claims 5, 6 and 21, Figure 4 of Hashimoto et al. discloses a semiconductor device, which includes: a first transistor (P-channel transistor 92), a second transistor (N-channel transistor 94), a third transistor (P-channel transistor 96), a fourth transistor (N-channel transistor 90), a first power source (100) applying a first potential (power supply such as Vdd), a second power source (ground) applying a second potential (ground), a first circuit (130, 134) for applying a third potential (Vy) which is different from the first potential and the second potential, a second circuit (114, 116) for generating a fourth potential (Vx) which is different from the first potential and the second potential, a first signal (signal at node 38), a second signal (signal at node 34) with the connections as recited in the claims.

With respect to claims 19 and 20, it is old and well known in the art that a transistor, when turning on, forms a resistor, and during the operation of the circuitry in Figure 4 of Hashimoto et al., the transistors 114 and 116 in the voltage divider circuit (114, 116), and the transistors 130 and 114 in the voltage divider (130, 134) are ON, so each of the transistors 114, 116, 130 and 134 forms a resistor. Thus, the circuit (114, 116) and the circuit (130, 134) each includes multiple resistors connected in series between the first power source (supply Vdd of the circuit) and the second power source (ground) and a potential is outputted from the connecting node of two resistors of each circuit.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
7. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816